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10/038,431	12/31/2001	Sushma Shrikant Trivedi	04860.P2687	7868

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
05/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/038,431	TRIVEDI ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 Feburyar 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-18,20-32 and 34-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18,20-32 and 34-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-18, 20-32, and 34-41 are pending. Claims 1, 12, 23, 25, and 26 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as filed 05 February 2008 and Amendment as filed 05 February 2008..

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier).

5. Regarding claims 1, 12, 23, 25, and 26, taking claim 1 as exemplary, Chehrazi has taught a method for execution by a microprocessor in response to receiving a single instruction (Chehrazi Col.20 lines 42-52), the method comprising:

a. Receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the register file (Chehrazi 310 of Fig.20B, Col.20 line 62 – Col.21 line 1);

b. Selecting a first plurality of numbers of the first vector from the first entry (Chehrazi 310 of Fig.20B, Col.20 line 62 – Col.21 line 1) and a second plurality of numbers of the second vector from the second entry (Chehrazi 312 of Fig.20B, Col.20 line 62 – Col.21 line 1) according to a configuration specified by the instruction (Chehrazi 560 of Fig 20A, Col.20 line 42 – Col.21 line 13), and

c. Generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers (Chehrazi Col.21 lines 6-12),

d. Wherein the sum of third plurality of numbers are saved in a third entry in the register file (Chehrazi Col.20 lines 47-58),

e. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (Chehrazi Col.20 lines 42-52, 61-62).

6. Chehrazi has not explicitly taught wherein the third plurality of numbers themselves are saved in an entry in a register file. However, Mennemeier has taught storing a third plurality of numbers, specifically a vector of absolute differences, in a instruction specified register (Mennemeier, Col.7 line 64 – Col.8 line 23) so that the absolute differences can be used in other operations that require the distance assessment that the results represent (Mennemeier, Col.8 line 21-23). One of ordinary skill in the art would have recognized that it is desirable to retain results that will be used by future instructions so that the results don't need to be recalculated. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chehrazi to store the absolute differences, rather than the sum of the absolute differences, in an

instruction specified register so that the values could be reused by other operations that require the data, thus improving throughput by avoiding the recalculation of the data.

7. Claims 12, 23, 25, and 26 are nearly identical to claim 1. However, Chehrazi has taught the differences. Claim 12 differs in the claim being comprised within a machine-readable media (Chehrazi Col.20 lines 42-46), while claims 23, 25, and 26 differs in the claims being comprised within an execution unit (Chehrazi Col.7 lines 20-40). Also, claim 23 claims wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54). Besides these differences, the claims encompass the same scope as claim 1. Thus, claims 12, 23, 25, and 26 are rejected for the same reasons as claim 1.

8. Regarding claims 2, 13, 24 and 27, taking claim 2 as exemplary, Chehrazi has taught a method as in claim 1, wherein an absolute difference between a first number and a second number is computed using a method comprising:

a. Producing a first intermediate number by subtracting the second number from the first number (Chehrazi Col.21 lines 1-8),

b. Producing a second intermediate number by subtracting the first number from the second number (Chehrazi Col.21 lines 1-8),

c. Selecting a positive number from the first intermediate number and the second intermediate number as the absolute difference between the first number and the second number (Chehrazi Col.21 lines 8-12),

d. Wherein the microprocessor is a media processor (Chehrazi 108 of Fig.1, Col.3 lines 6-7) disposed on an integrated circuit with a memory controller (Chehrazi 100 of Fig.1, Col.5 lines 46-54).

9. Claims 13, 24 and 27 are nearly identical to claim 2. Claim 13 lacks the recitation of a media processor disposed on an integrated circuit with a memory controller, and claims 13, 24 and 27 differ in their parent claims, but encompass the same scope as claim 2. Thus, claims 13, 24 and 27 are rejected for the same reasons as claim 2.

10. Regarding claims 3, 14 and 28, taking claim 3 as exemplary, Chehrazi has taught a method as in claim 2, wherein the first intermediate number and the second intermediate number are produced in parallel (Chehrazi Col.21 lines 1-8), and wherein the third plurality of numbers are generated substantially simultaneously (Chehrazi Col.21 lines 8-12).

11. Claims 14 and 28 are nearly identical to claim 3, both differing in their lack of having the third plurality of numbers being generated substantially simultaneously, as well as differing in their parent claims, but both encompass the same scope as claim 3. Thus, Claims 14 and 28 are rejected for the same reasons as claim 3.

12. Regarding claims 5, 16 and 30, taking claim 5 as exemplary, Chehrazi has taught a method as in claim 1, wherein the first plurality of numbers are received from a first entry in the register file (Chehrazi Col.20 lines 47-58).

13. Claims 16 and 30 are nearly identical to claim 5, differing in their parent claims, but encompassing the same scope as claim 5. Thus, claims 16 and 30 are rejected for the same reasons as claim 5.

14. Regarding claims 6, 17 and 31, taking claim 6 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies a way to partition a string of bits in the first entry into a first plurality of numbers (Chehrazi Col.20 lines 61-65). Here, the SABD

instruction specifies a register in the register file, which corresponds to the plurality of numbers, and specifies that the data in the register be interpreted to be 16 separate 8-bit numbers.

15. Claims 17 and 31 are nearly identical to claim 6, differing in their parent claims, but encompassing the same scope as claim 6. Thus, claims 17 and 31 are rejected for the same reasons as claim 6.

16. Regarding claims 7, 18 and 32, taking claim 7 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies an index of the entry in the first register file (Chehrazi 560c and 560d of Fig.20a, Col.20 lines 47-58).

17. Claims 18 and 32 are nearly identical to claim 7, differing in their parent claims, but encompassing the same scope as claim 7. Thus, claims 18 and 32 are rejected for the same reasons as claim 7.

18. Regarding claims 9, 20 and 34, taking claim 9 as exemplary, Chehrazi in view of Mennemeier has taught a method as in claim 1, wherein the single instruction specifies an index of the entry in a the register file (Mennemeier, Col.7 line 64 – Col.8 line 23, as well as above paragraph 39).

19. Claims 20 and 34 are nearly identical to claim 9, differing in their parent claims, but encompassing the same scope as claim 9. Thus, claims 20 and 34 are rejected for the same reasons as claim 9.

20. Regarding claims 10, 21 and 35, taking claim 10 as exemplary, Chehrazi has taught a method as in claim 1, wherein a type of each of the first and second pluralities of numbers is one of:

a. Unsigned integer (Chehrazi Col.20 lines 54-55),

b. Signed integer (Chehrazi Col.20 lines 54-55),

c. Floating-point number.

21. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 10.

22. Claims 21 and 35 are nearly identical to claim 10, differing in their parent claims, but encompassing the same scope as claim 10. Thus, claims 21 and 35 are rejected for the same reasons as claim 10.

23. Regarding claim 11, 22 and 36, taking claim 11 as exemplary, Chehrazi has taught a method as in claim 1, wherein a size of each of the first and second pluralities of numbers is one of:

a. 8 bits (Chehrazi Col.20 lines 61-65),

b. 16 bits,

c. 32 bits.

24. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 11.

25. Claims 22 and 36 are nearly identical to claim 11, differing in their parent claims, but encompassing the same scope as claim 11. Thus, claims 22 and 36 are rejected for the same reasons as claim 11.

26. Regardin claim 37, Chehrazi has taught wherein a type of each of the first and second pluralities of numbers is floating point number (Chehrazi column 1, lines 19-21 and column 9, lines 37-41).

27. Regarding claim 38, Chehrazi has taught wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54).

28. Regarding claim 40, Chehrazi has taught wherein the memory controller is usable to access memory not disposed on the integrated circuit (Chehrazi Col. 5 lines 36-60 and Figure 1). As can be seen in Chehrazi's Figure 1, the ROM and RAM memories and data storage device are separate from the processor.

29. Regarding claim 41, Chehrazi has taught wherein the memory controller is usable by a host central processing unit not disposed on the integrated circuit to access the memory (Chehrazi Col. 5 lines 36-60 and Figure 1). As can be seen in Chehrazi's Figure 1, the ROM and RAM memories and data storage device are separate from the processor.

30. Claims 4, 15, 29, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier) as applied to claims 1, 2, 12, 26, and 27 above, and further in view of Diefendorff et al., EPO 0 485 776 A2 (herein referred to as Diefendorff).

31. Regarding claims 4, 15, 29, and 39, taking claim 4 as exemplary, Chehrazi has taught taking an absolute difference between a first number and a second number (Chehrazi Col.21 lines 6-12). Chehrazi has not taught:

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number,

b. Saturating the difference between the first number and the second number if an overflow occurs.

32. Diefendorff has taught

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5),

b. Saturating the difference between the first number and the second number if an overflow occurs (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5).

33. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Diefendorff, that overflow testing and saturation arithmetic improves the handling of overflow conditions during shading or image processing, thereby improving the quality of the image and accelerating the performance of the microprocessor during shading and image processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the overflow testing and saturation arithmetic of Diefendorff in the device of Chehrazi to improve image quality and accelerate the performance of a microprocessor during shading and image processing.

Response to Arguments

34. Applicant's arguments filed 05 February 2008 have been fully considered but they are not persuasive. Applicants' argue in essence on pages 13-17

> ...Chehrazi merely discloses a first input register (310) that stores a [vector[of operands Vt and a second input register (312) that stores a [vector] of operands Vs

(Figure 20B). In contrast, amended claim 1 refers to receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second ent6ry in the same register file.

Further, Chehrazi merely discloses computing the differences between corresponding operands stored in the operand registers, Vt and Vs. In contrast, amended claim 1 refers to selecting a first plurality of numbers of the first vector from the first entry and a second plurality of numbers of the second vector of numbers of the second vector from the second entry according to a configuration specified by the instruction.

Additionally, Chehrazi merely discloses a third destination register Vd that stores the sum of absolute differences of operands from the first and second registers. In contrast, amended claim 1 refers to generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, wherein the third plurality of numbers are saved in a third entry in the register file.

35. This has not been found persuasive. A register file is an array of registers in a processor. In Chehrazi, the register file contains both the operand registers and the register the result is written to. Therefore, the operands and result are a first, second, and third entry in a register file. Also, the SABD instruction selects the operands by which register in the register file are used. In fact, the SABD selects to use all of the numbers in the operand registers. Consequently, the SABD instruction selects entire vectors from the registers they are stored in.

Conclusion

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183
26 May 2008